White Paper
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TI BAW technology enables ultra-low jitter clocks for high-speed networks

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1 Introduction

DPLL (Digital Phase-Locked Loop) based network synchronizers, which generate and distribute clean output clocks to various sub-systems based on received network clocks, are critical components in communication network equipment. The simplified diagram in Figure 1 demonstrates how network synchronizers are used in timing cards and line cards of typical communication equipment such as routers and switchers. To comply with requirements of communication standards such as ITU-T G.8262, network synchronizers are used to detect valid input clocks, filter input clock wander, and perform hitless switching and holdover functions. Low noise clocks are generated based on APLL's (Analog Phase-Locked Loop) locked to an external crystal reference oscillator (XO), or a temperature-compensated XO (TCXO) or an oven-stabilized XO (OCXO).

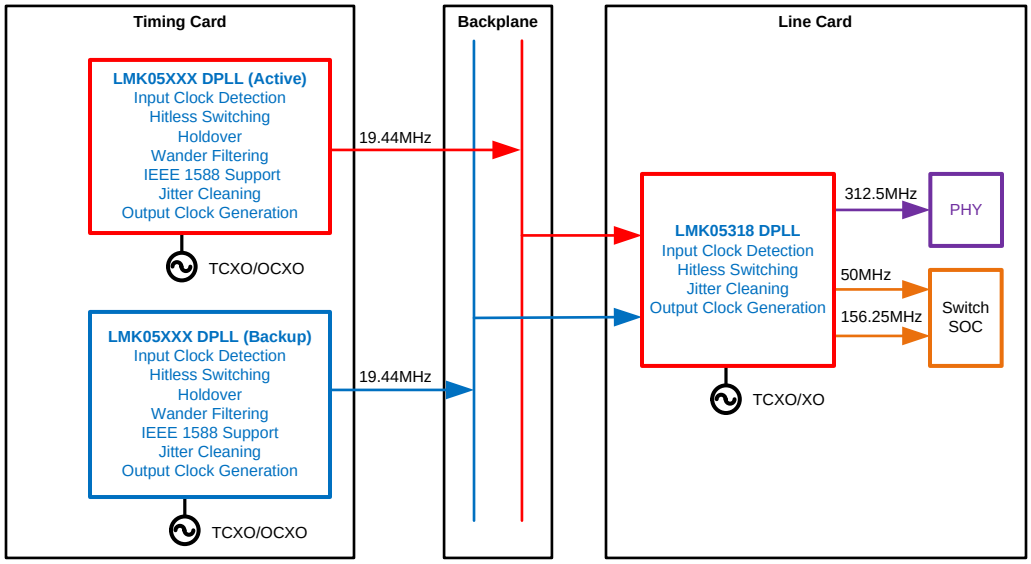

Figure 1. Simplified diagram for network synchronizers used in communication equipment timing cards and line cards.

One key specification for network synchronizers is output clock integrated root-mean-square (rms) jitter, which is integrated over a certain frequency band specified by various communication standards. The required network synchronizers output clock jitter is becoming more and more challenge to meet stringent signal noise ratio (SNR) / bit error rate (BER) requirement and have good design margins as communication network data rates continue to increase due to explosive data traffic growth. For example, as communication networks evolve from 100 Gigabits per second (Gbps) to 400 Gbps systems, system designers require that network synchronizers output clocks maximum total rms jitter integrated from 12kHz to 20MHz (TJrms_12kHz_20Mhz, including spurs) to be less than 150fs. For simplicity, in the following discussion of output clock total rms jitter, the integration bandwidth is always from 12kHz to 20Mhz and spurs are always included.

The state-of-the-art network synchronizer IC's typically generate output clocks based on an integrated high frequency LC VCO. The VCO phase noise is limited by quality factor of its integrated LC tank, typically around 20~30 after optimization. Assuming the LC VCO is locked by a PLL with a very narrow loop bandwidth such as 100Hz, the output clock rms jitter could be around several hundred fs or higher, mainly dominated by LC VCO phase noise, thus unable to meet 150fs requirement.

To achieve better rms jitter, designers can increase the APLL loop bandwidth to attenuate close-in phase noise from a VCO. However, due to the analog nature of fractional-N APLL, the APLL inherent in-band phase noise is limited by analog imperfections and may be sensitive to process, supply, temperature (PVT) variations as well as crosstalk effects. The crystal reference oscillator phase noise is also limited. As a result increasing APLL loop bandwidth beyond certain range may cause APLL inherent in-band phase noise and crystal reference oscillator phase noise to become the dominant contributors thus preventing further reduction of total rms jitter. Furthermore, increasing APLL loop bandwidth also degrades filtering of fractional-N spurs and quantization noise thereby may degrade total rms jitter performance.

With a low noise high frequency (such as 48Mhz) XO, the optimum PLL loop bandwidth for minimum rms jitter could typically be a few hundred kHz or higher for state-of-the-art network synchronizer IC's utilizing LC VCO's, which results in maximum total rms jitter around 150fs or higher. For these reasons the conventional network synchronizers based on LC VCO are becoming the performance bottleneck for 400-Gbps and future higher speed communication systems.

Another drawback of conventional network synchronizers based on LC VCO is their requirement of a high frequency low noise crystal reference oscillator for total rms jitter optimization. To meet stringent holdover accuracy requirements for certain systems, such as max +/- 4.6ppm as specified for Sync E in ITU-T G.8262, a TCXO or OCXO is preferred over a normal un-compensated XO. However, reliable high frequency low noise TCXO's or OCXO's are not easily available and are usually expensive. Therefore system designers have to make trade-off's among clock phase noise/jitter performance, holdover accuracy, and total solution cost.

To solve this challenge issue, designers can utilize the LMK05318 network synchronizer IC solution that features a Bulk Acoustic Wave (BAW) technology. This device uses a high-Q BAW resonator co-packaged with silicon IC to implement an ultra-low noise integrated Voltage-Controlled BAW Oscillator (VCBO). As shown in the following, the 2.5GHz VCBO close-in (1kHz~100kHz) phase noise is about 10~20dB better than the state-of-the-art LC VCO. The innovative BAW technology greatly reduces the synchronized output clock phase noise/rms jitter thereby meeting the challenge requirement of max rms jitter less than 150fs with comfortable margin, which exceeds 400-Gbps system requirements and allows future migration to data rates above 400-Gbps. Additionally, this solution lowers overall solution cost by eliminating the need for a high frequency low noise TCXO or OCXO.

2 Ultra-Low Noise Voltage-Controlled BAW Oscillator IP

BAW resonators featuring high operating frequency up to a few GHz and small size have been used for mobile applications such as filters in the RF front-end of wireless transceivers for many years. The BAW resonator is a piezoelectric thin film resonator, which operates similarly to a quartz crystal. As shown in Figure 2, a piezoelectric thin film is sandwiched between two metal electrodes and several acoustic reflectors to confine mechanical energy. The end result is a very stable high-Q resonator tank.

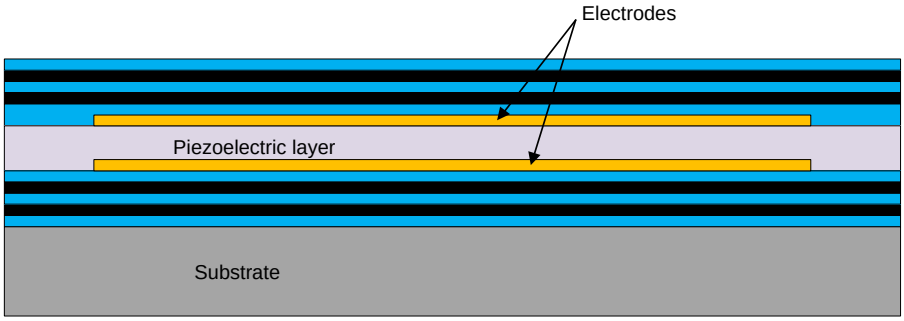

Figure 2. Basic structure of a Bulk Acoustic Wave (BAW) resonator.

The electrical equivalence of a BAW resonator can be represented by a modified Butterworth-Van Dyke (MBVD) model, as shown in Figure 3. Like a conventional crystal resonator, it has a parallel resonance frequency Fp and serial resonance frequency Fs.

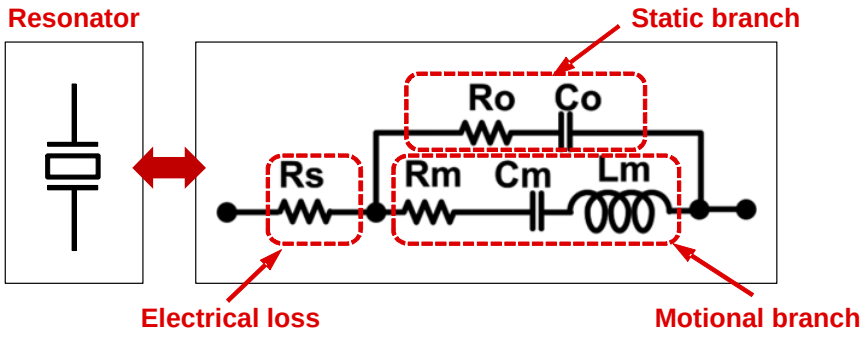

Figure 3. The modified Butterworth-Van Dyke (MBVD) model, electrical equivalent of a BAW resonator

Through many years of joint research and development efforts among various functional teams within the company, TI has perfected the recipe for a high frequency high-Q BAW resonator while simultaneously solved the challenge of co-packaging it with silicon IC. The typical quality factor of a BAW resonator used in 2.5GHz VCBO is 1200.

The total rms jitter of a typical 2.5GHz VCBO based on TI's innovative BAW technology is around 33fs at 1.25Ghz output, as shown in Figure 4. Comparison results of phase noise performance of LMK05318 2.5GHz VCBO with the state-of-art LC VCO of LMX2582 (normalized to 2.5GHz) are shown in Figure 5 and Table 1. The 2.5GHz VCBO close-in (1kHz~100kHz) phase noise is about 10~20dB better than the state-of-the-art LC VCO, which clearly demonstrates the phase noise/jitter advantage of VCBO. Based on this superior low phase noise VCBO technology, ultra-low jitter network synchronizer products like LMK05318 are developed to meet challenge requirements of advanced high speed communication networks such as 400Gbps systems.

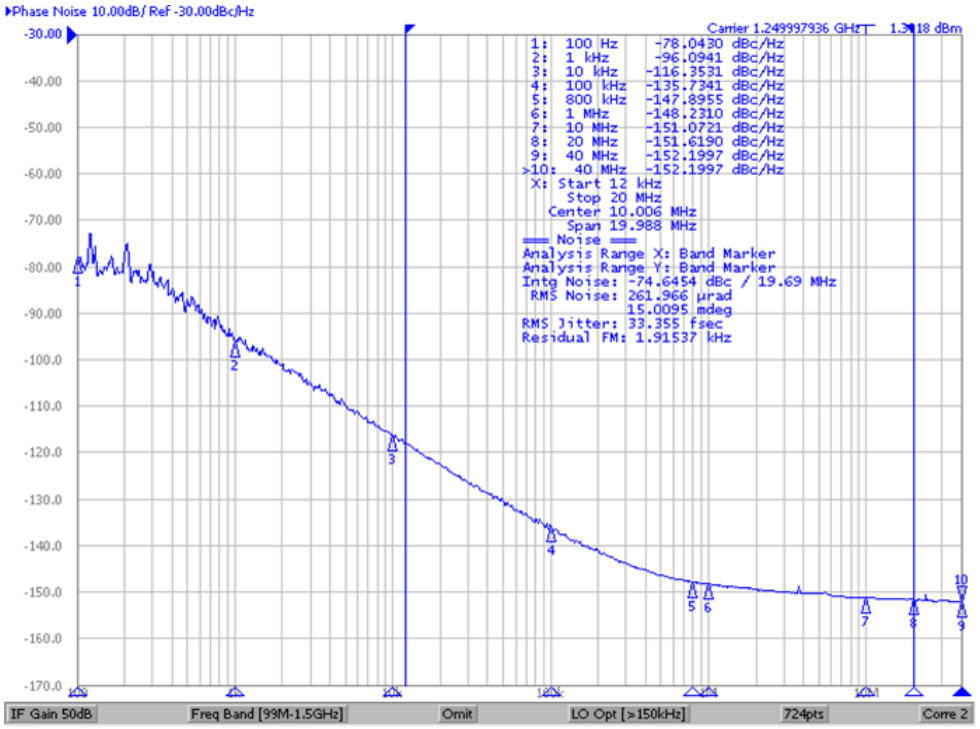

Figure 4. Typical 2.5GHz VCBO phase noise (measured at a carrier frequency of 1.25GHz). The total rms jitter is around 33fs.

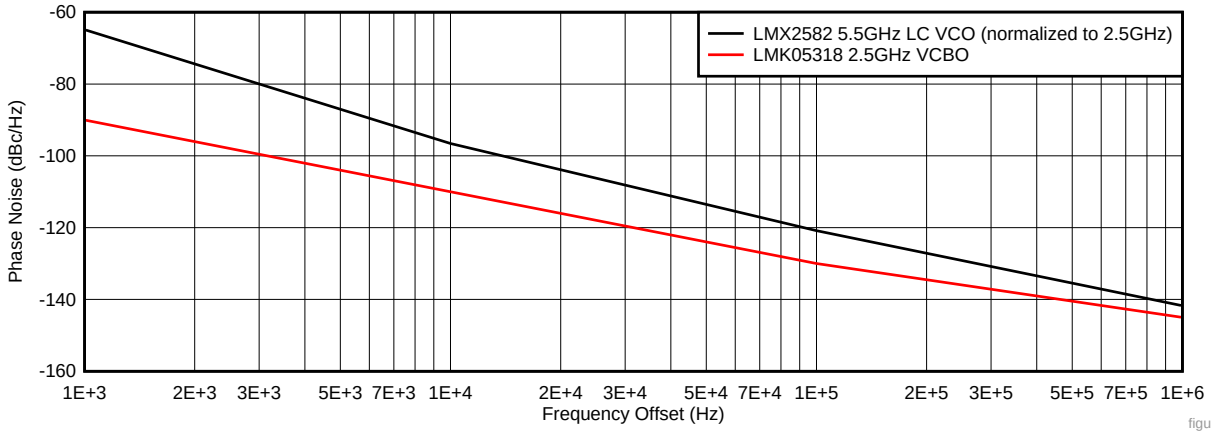

Figure 5. Compare phase noise performance of LMK05318 2.5GHz VCBO with the state-of-art LC VCO of LMX2582 (normalized to 2.5GHz)

Table 1. Compare phase noise performance of LMK05318 2.5GHz VCBO with the state-of-art LC VCO of LMX2582 (normalized to 2.5GHz) .

Offset Frequency (Hz)	LMX2582 5.5GHz LC VCO (normalized to 2.5GHz) (dBc/Hz)	LMK05318 2.5GHz VCBO (dBc/Hz)	Improvement (dB)
1k	-64.8	-90	25.2
10k	-96.5	-110	13.5
100k	-120.8	-130	9.2
1M	-141.7	-145	3.3

3 LMK05318 Ultra-Low Jitter Network Synchronizer Chip Architecture

LMK05318 is the industry's first commercial network synchronizer that utilizes a high frequency high-Q BAW resonator integrated in a standard QFN package together with the silicon IC to form a VCBO to generate ultra-low jitter clocks. The chip level block diagram of the LMK05318 ultra-low jitter network synchronizer is shown in Figure 6.

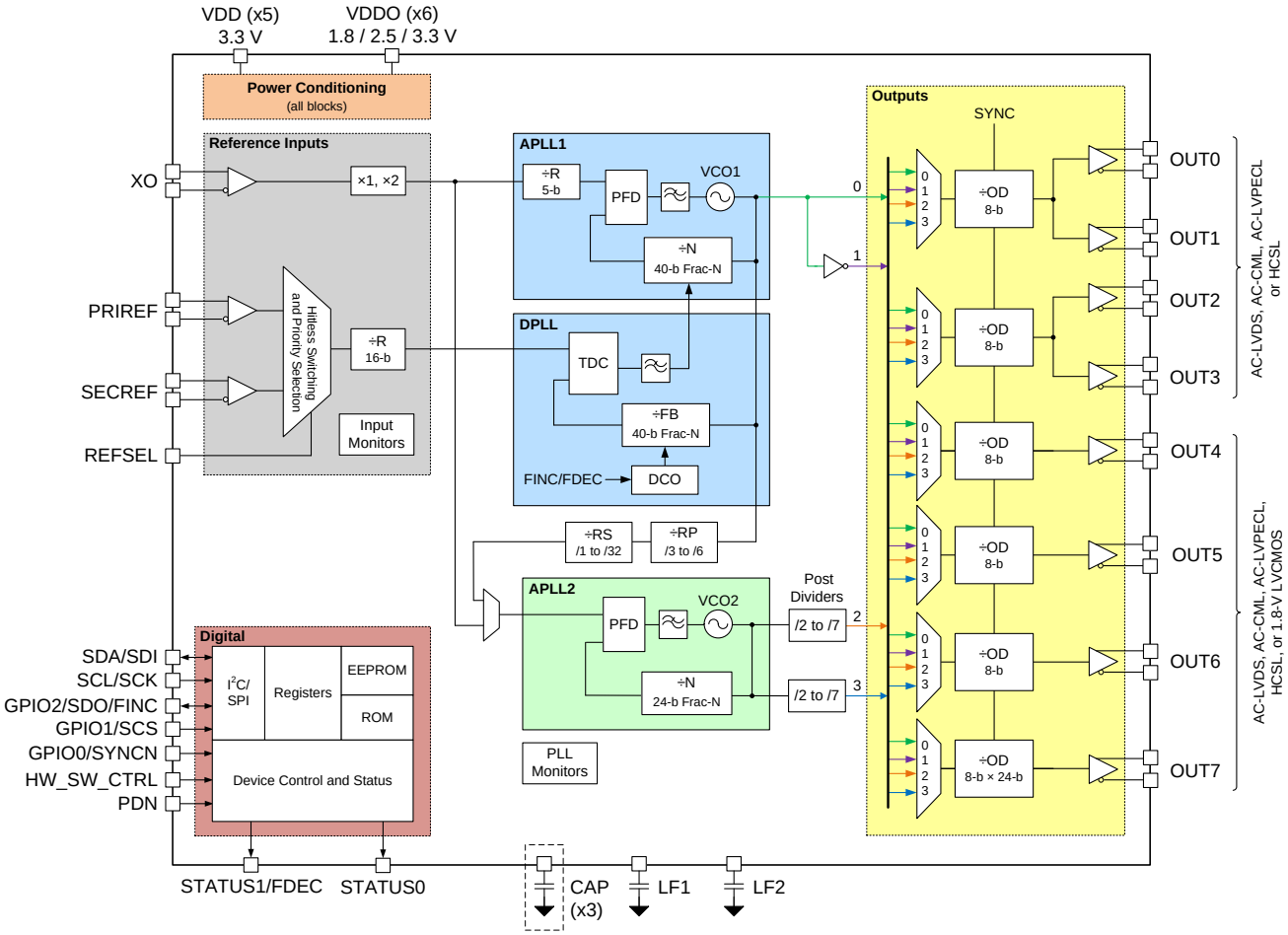

Figure 6. LMK05318 simplified chip level block diagram.

LMK05318 has a fully programmable DPLL core, which provides input clock detection/monitoring, wander/jitter filtering, and supports industry's best hitless input clock switching and holdover functionality. The device can operate in normal operation mode with DPLL enabled, holdover mode with input clocks disabled, or free run mode. LMK05318 meets requirements of various communication standards such as ITU-T G.8262. Features such as on-chip EEPROM, on-chip LDO's, make it easy to configure and operate the device. Refer LMK05318 datasheet for many other useful features.

The VCO1 of APLL1 is a 2.5GHz VCBO. Output clocks generated from APLL1 achieves industry's best-in-class output clock rms jitter and phase noise performance. As shown in the following Figure 7, the 312.5Mhz output typical total rms jitter is around 47fs.

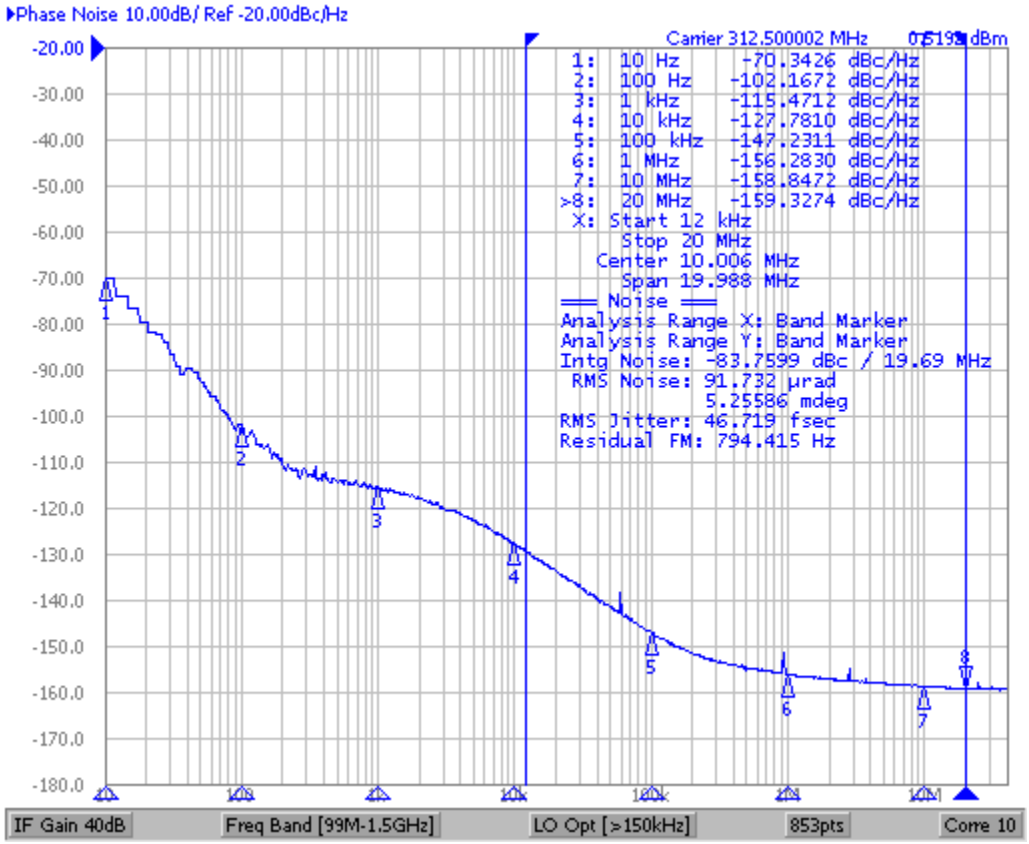

Figure 7. Typical DPLL/APLL1 312.5Mhz output phase noise. TJrms_12_20Mhz is around 47fs.

APLL2 with a 5.5~6.25GHz LC VCO can be used to generate clocks that cannot be generated from 2.5GHz VCBO directly. For 155.52Mhz output from APLL2, total rms jitter is around 118fs.

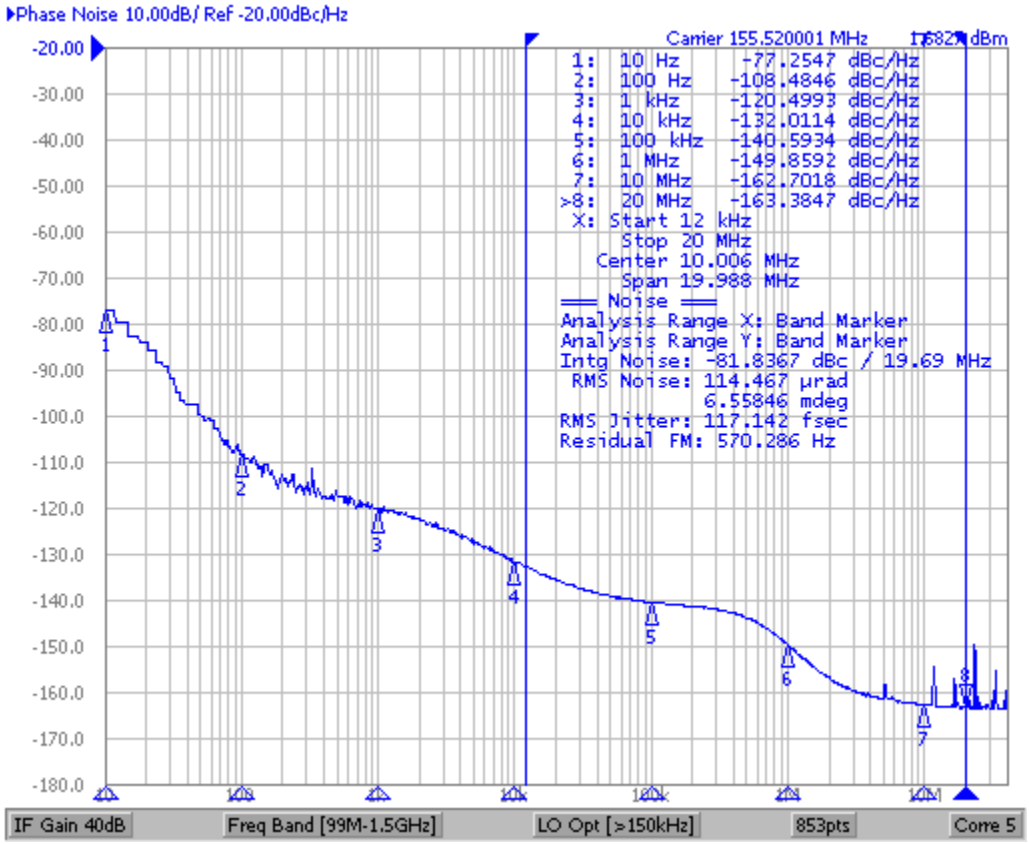

Figure 8. Typical APLL2 155.52Mhz output phase noise. FVCO2=5598.72Mhz, APLL2 FPD=2500Mhz/18=138.8…Mhz. TJrms_12_20Mhz is around 118fs.

Additional benefits of LMK05318 solution with a VCBO are summarized in Table 2 and discussed in the following.

4 Better Mid-Band Phase Noise (10kHz~1MHz)

As shown in Figure 9, the mid-band phase noise (10kHz~1MHz) of LMK05318 is much better than conventional solutions based on LC VCO's since it is mainly dominated by VCBO close-in phase noise and there is no big noise hump contributed by wide-band APLL1,. This is a big advantage in systems such as wireless cellular macro base-stations that require stringent clock mid-band phase noise at certain frequency offsets (like MC-GSM phase noise at 800kHz offset, etc).

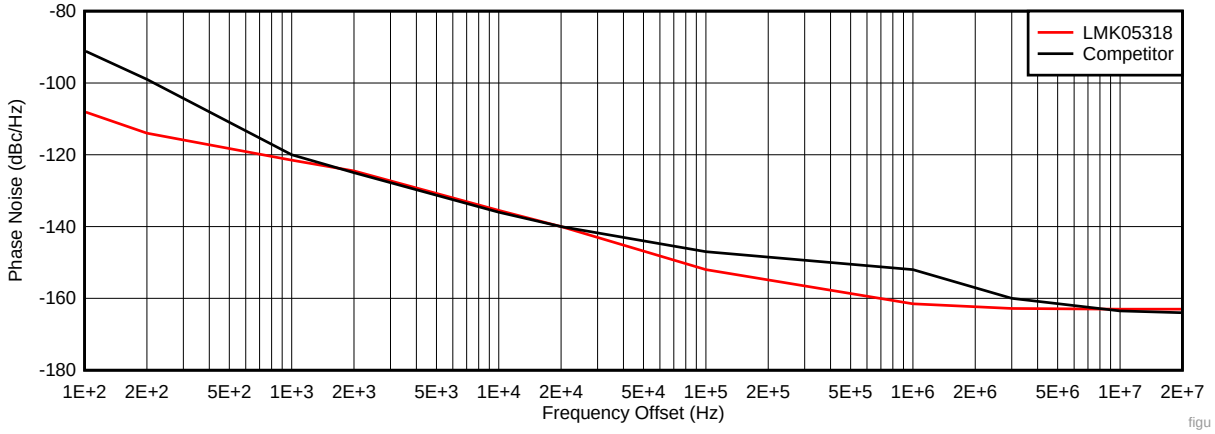

Figure 9. CLKout phase noise comparison of LMK05318 with conventional LC VCO based network synchronizers from competition.

5 Allow Usage of Low Frequency TCXO/OCXO/XO to Reduce Total Solution Cost

Thanks to the ultra-low noise VCBO, it can be observed from Figure 7 that the ultra-low jitter of LMK05318 output clocks is achieved with APLL1 loop bandwidth of a few kHz, which implies external XO/TCXO/OCXO phase noise has less impact for total rms jitter. Low frequency (like 10~20MHz) TCXO/OCXO/XO may be used for LMK05318 without significant impact to total rms jitter, thereby lowering total solution cost.

As a comparison, the conventional solution requires high frequency (around 50MHz) external TCXO/OCXO/XO's with low phase noise that are typically more expensive.

6 More Reliable Phase Noise and Total rms Jitter

There are a few reasons that LMK05318 output clock total rms jitter is less susceptible to Process, Supply, Temperature (PVT) variations. First, LMK05318 output clock total rms jitter is mainly dominated by VCBO phase noise and insensitive to APLL in-band phase noises and external TCXO/OCXO/XO phase noise. As a comparison, for conventional solution using wide-band APLL with LC VCO, its total rms jitter is sensitive to APLL in-band phase noise and external TCXO/OCXO/XO phase noise. Note in-band phase noise of fractional APLL is sensitive to modulation nonlinearities so that it can vary quite a lot over PVT variations.

Second, for conventional solution, the wide loop bandwidth (at least several hundred kHz) of APLL makes it more difficult to filter out fractional spurs and fractional PLL quantization noise. In contrast, for LMK05318 with narrow loop bandwidth APLL (a few kHz), the fractional spurs and fractional PLL quantization noise can be easily filtered out resulting lower output clock phase noise/jitter.

Table 2. Benefits of LMK05318 Network Synchronizer with a 2.5GHz VCBO when compared with conventional solution with an LC VCO

Factors	Network Synchronizer Based VCBO	Network Synchronizer Based LC VCO
APLL FPD frequency	Low FPD can be used (a few MHz or lower) and still achieve good rms jitter	High FPD (about 50 MHz or higher) is required to achieve good rns jitter
APLL loop bandwidth for optimum total rms jitter (12 kHz to 20 MHz)	Narrow (below a few kHz)	Wide (above a few hundred kHz)
Mid-band phase noise	Superior mid-band phase noise (10 kHz to ~1 MHz)	Worse mid-band phase noise due to noise contribution of wideband APLL
Max total rms jitter (12 kHz to 20 MHz)	100 fs or less	150 fs or higher
APLL in-band phase noise variation over PVT	Total rms jitter is less sensitive to APLL in-band phase noise over PVT	Total rms jitter is sensitive to APLL in-band phase noise over PVT
APLL fractional spurs and quantization noise over PVT	Lower APLL fractional spurs and quantization noise due to more filtering of narrowband APLL	Worse APLL fractional spurs and quantization noise due to less filtering of wideband APLL
Cost of reference crystal oscillator	Can use normal low-frequency TCXO/OCXO/XO to reduce overal solution cost	Need expensive low-noise high-frequency TCXO/OCXO/XO to achieve good rms jitter

7 Conclusions

The required network synchronizers output clock jitter is becoming more and more challenging for conventional solutions based on LC VCO to achieve as communication network data rates keep going higher. A new network synchronizer solution LMK05318 based on the break-through BAW technology was developed to significantly improve phase noise / rms jitter performance over conventional solutions based on LC VCO. The BAW resonator is manufactured in a CMOS-compatible process and is integrated with the silicon IC die in a standard QFN package. The 2.5GHz VCBO close-in (1kHz~100kHz) phase noise is about 10~20dB better than the state-of-the-art LC VCO, which clearly demonstrates the phase noise/jitter advantage of VCBO. The output clock typical total rms jitter is 33fs at 1250MHz output and is 47fs for 312.5Mhz output. The output clock maximum total rms jitter is less than 100fs, exceeding stringent rms jitter specification required for high speed 400-Gbps communication networks. Unlike conventional approach based on a LC VCO, a lower frequency lower cost normal TCXO/OCXO can be used with LMK05318, which reduces total solution cost. Additional benefits of LMK05318 network synchronizer with a 2.5GHz VCBO are summarized in Table 2.

8 Additional Information

Here is more information from TI on the Ultra Low Jitter Network Synchronizer Product SNAS771.

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